THEORETICAL AND EXPERIMENTAL INVESTIGATION OF BIAS AND TEMPERATURE EFFECTS ON HIGH RESISTIVITY SILICON SUBSTRATES FOR RF APPLICATIONS

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ABSTRACT

Theoretical and experimental comparisons show that the RF characteristics of the a CPW in Schottky contact with a HR Si substrate are bias independent for all practical temperatures, upto 100 ˚C. Bias dependence on the RF characteristics of the transmission line are noticed above 100 ˚C when the ohmic dielectric loss of the HR Si becomes the dominant loss mechanism on the coplanar structures under study. This is a direct result of the increase of intrinsic carrier density.

I. BACKGROUND

It was demonstrated in [1] that commercially available low-cost HR Si with resistivities greater than 3 k Ω-cm can be used as a microwave substrate. The comparative experiments in [1] were carried out at 25 °C and zero DC bias on Schottky contact coplanar waveguides (CPW) and on Schottky contact inductive coplanar structures like meanders and single layer spiral inductors. However, results reported in [2] indicate that the attenuation of a microstrip transmission line on HR Si is dependent on the applied DC bias. Results of studies dealing with the impact of temperature and DC bias on low-cost low-loss HR Si substrate were reported on [3]. This study reports no dependency on applied DC bias on the RF characteristics of coplanar structures (CPW and meander inductor) in Schottky contact with the HR Si substrate from -50 ˚C to 100 ˚C. In this paper, we explain through semiconductor device simulations with emphasis on the CPW transmission line the reasons why the Schottky coplanar structures on HR Si substrate have no DC bias dependence on their RF characteristic upto 100 ˚C.

The impact of Si dielectric losses on microstrip transmission lines as a function of temperature have been theoretically analyzed by Sobol [4] and Rosen [5]. Temperature effects were investigated experimentally by Taub [6] on CPW transmission line on none-commercially available HR Si with resistivities in the 30 k Ω-cm range which is almost an order of magnitude higher than the one under study in this paper. As previously mentioned, bias dependence experimental work has been done by Levesque [2] but this was done on microstrip transmission lines. This paper presents both theoretical and experimental analysis of the semiconductor losses when high resistivity silicon is used as a substrate for RF applications. The new research includes measurements and simulations demonstrating that the RF characteristics of the CPW in Schottky contact with the HR Si Substrate are bias independent only upto 100 ˚C. Bias dependence on the RF characteristics of the transmission line are noticed above 100 ˚C when the ohmic dielectric loss of the HR Si becomes the dominant loss mechanism on the coplanar structures under study due to the increase of intrinsic carrier density.

II. STRUCTURES FABRICATED AND DESCRIPTION OF THE EXPERIMENT

Fig. 1. shows the top view of the CPW under study. Cross-section of the CPW is shown in Fig. 2. The CPW's line width "w" is 30 μm, line spacing "s" is 10 μm, and the line length is 1000 μm. The substrate thickness "h" of the HR Si substrate is 400 μm. The HR N type Si substrate has a (111) crystal orientation. The substrate resistivity at room temperature is between 3000 to 7000 Ω-cm. Electroplated gold is used to pattern the 2.5 μm of metal thickness. The metal system in Schottky contact with the HR Si is sputtered TiW. Maximums barrier heights of 0.50 and 0.67 eV are achieved for Ti and W respectively [7]. The maximum barrier height for the TiW alloy is somewhere between 0.50 and

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0.67 eV. However, it is expected that the barrier height is lowered since the deposition process of TiW is optimized for Si_3N_4 and no for Schottky contact with Si.

. The temperature setting used were: 150, 100, 50, 25, 0 -25, and -50 °C. At each temperature setting, the DC bias was applied to the devices fabricated on the HR Si. The voltage was varied as follows: 10, 6, 3, 1.5, 0, -1.5, -3, -6, and -10 volts. The DC bias was applied to the coplanar structures through port 1 of the Vector Network Analyzer. In order to take into account process variability across the wafer, five samples were measured for each coplanar structure at each setting. The two port S parameter measurements were averaged. The averaged S parameter were translated into attenuation constant "α" and phase constant "ß" using the Even and Odd mode method [9]. The quality factor of the transmission line is defined as "Q" = ß / 2 α.

III. DEVICE SIMULATION

The commercially available device simulator ATLAS™ from SILVACO International is used to simulate the CPW structure on the HR Si substrate for various temperature and DC bias conditions. The temperature is varied from 25 ˚C to 150 ˚C in increments of 25 ˚C. The DC bias is varied from -10 V to 10 V in increments of 5 V. The cross-section of the simulated structure is similar to the one described in Fig. 1. The simulated structure has the following features: 1) substrate thickness is 150 μm; and 2) ground plane width is 150 μm. An initial grid of 2.5 μm by 2.5 μm is used in a cross-sectional area of 100 μm by 100 μm under the center conductor. The reminder of the substrate is initially set up for a grid of 10 μm by 10 μm. The work function option of the contact statement is set to 4.61 eV based on a calibration study run with measured data. This work function (electron affinity is defined at 4.17 eV in ATLAS™) is equivalent to a barrier height of 0.46 eV which is 0.04 lowered than the maximum for Ti. The lower barrier height is explained by the process used to deposit the TiW which is optimized for dielectric layers and not for a Schottky contact for Si. The lower barrier height implies a higher leakage current. The barrier height lowering due to the electric field is taken into account in our simulation. The fixed surface charge is set to 10^{11} cm^{-2}. The background doping is set, based on substrate resistivity simulation results, to 10^{12} cm^{-3} for electrons and 10^{11} cm^{-3} for holes. The carrier mobility was taken as function of doping and the local electric field.

IV. RESULTS AND DISCUSSION

The CPW under study is in Schottky contact with the HR Si, it is expected that the Q of these structures are DC bias dependent. Fig. 3 shows the Q of the CPW on HR Si as functions of frequency at various bias setting at 25 °C. Fig. 3 indicates that there is no change in the Q of the CPW due to the bias change. Similar characteristics are observed for measurements at -50, -25, 0, and 50 ˚C. Simulated results are used to explain why there is no variation in the attenuation with the DC bias. Plotted on Fig. 4 are the electron and hole concentration under the conductor electrode for the CPW on the HR Si for a depth of 60 μm at 25 ˚C. The same carrier concentration profile is observed under the ground electrodes. Several interesting phenomena are observed. First, there is no apparent depletion width. It appears that the electron concentration is pinned to the doped concentration. Similarly, the hole concentration is also pinned but to the value that satisfies the charge neutrality. Therefore, there is very little bias dependence on the electron and hole concentrations.

At 100 °C, it is observed that the bias on the line starts to have a small effect on the losses. Fig. 5 shows that the Q at 10 and 3 volts is higher than the attenuation at -10 and -3 volts. The Q at 0 bias seems to be right in between the negative and positive bias. The bias dependence of the losses in Fig. 5 are explained with help of Fig. 6. Fig. 6 shows the simulated electron and hole concentration profile under the conductor electrode of the CPW on HR Si at 100 ˚C as a function of bias. The profile under the ground plane electrodes is the opposite bias wise to the one shown in Fig. 6. The electron concentration is higher for negative bias and lower for positive bias conditions. The electron concentration for zero bias is in between the electron concentration for positive and negative bias. The difference in the electron/hole concentrations between positive and negative bias can be explained through the charge neutrality equation, which can be approximated for the structure under study as

$$N_d + p = n \quad (1)$$

When the conductor is positively biased, the positive charges from the hole concentration are repelled and Equation 1 is reduced to

$$N_d \approx n \tag{2}$$

therefore, the hole concentration is given by

$$p = \frac{n_i^2}{n} \tag{3}$$

where n_i is the intrinsic carrier concentration. From Fig. 4, it can be observed that the electron concentration is approximately equal to dopant concentration. On the other hand, when conductor is negatively biased, the negative charges from N_d do not move because these are fixed charges. Therefore, equation (1) remains intact. There is no repelling of charges at 0 bias. Thus, equation (1) also applies to the 0 bias case.

At 150 ˚C, there is a clear distinction between the positive bias and the negative/zero bias cases. Fig. 7 shows the Q of the CPW on the HR. Si substrate at -10, -3, 0, 3, and 10 volts. The simulated electron and hole concentrations profiles under the conductor electrode at 150 ˚C are plotted in Fig. 8 for various bias conditions. The same Q behavior observed in the CPW measurement due to change in bias is also observed for the meander structure [3].

V. CONCLUSION

In this paper, we presented theoretical and experimental analysis of bias and temperature dependence of the HR Silicon substrates RF characteristics. The comparison showed that the RF characteristics of the CPW in Schottky contact with a HR Si substrates are practically bias independent for temperatures upto 100 ˚C. Bias dependence of the RF characteristics of the transmission line are noticed above 100 ˚C, when the ohmic dielectric loss of the HR Si becomes the dominant loss mechanism on the coplanar structures under study. It was demonstrated that this bias dependence is caused mainly by the increase of intrinsic carrier density.

VI. REFERENCES

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Fig. 1. CPW (Line Length = 1000 μm)

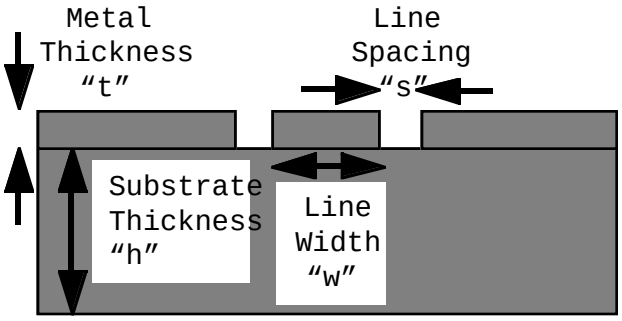

Fig. 2. Cross-Section of the CPW

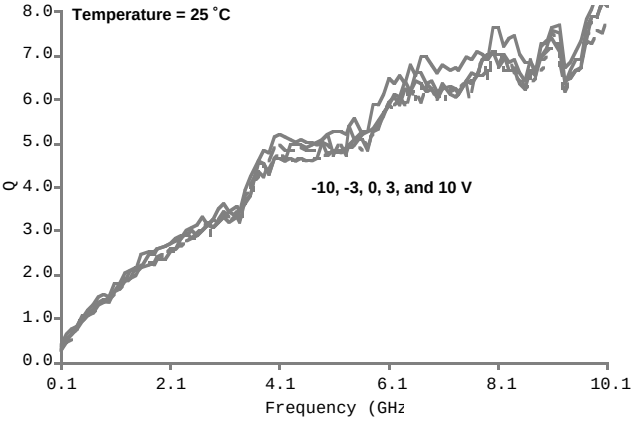

Fig. 3. Measured Q vs. Frequency of CPW at Various Bias Conditions at 25˚C

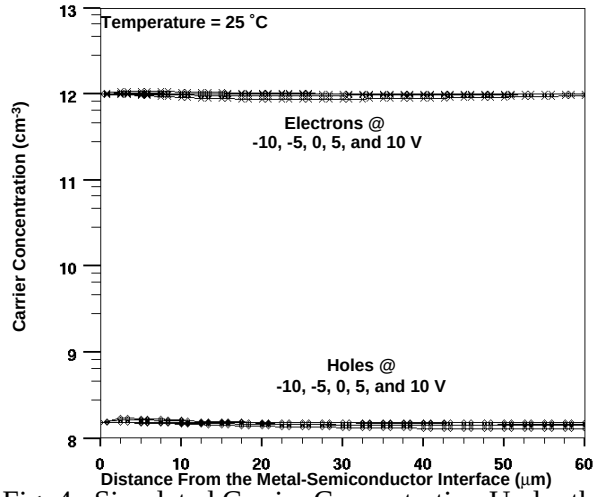

Fig. 4. Simulated Carrier Concentration Under the Conductor for Various Bias Conditons at 25 ˚C

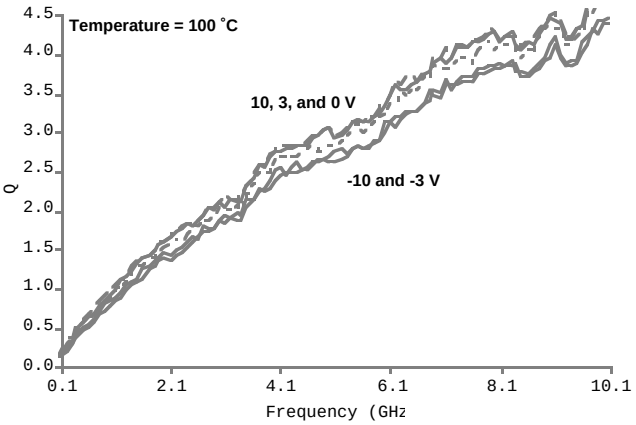

Fig. 5. Measured Q vs. Frequency of CPW at Various Bias Conditions at 100˚C

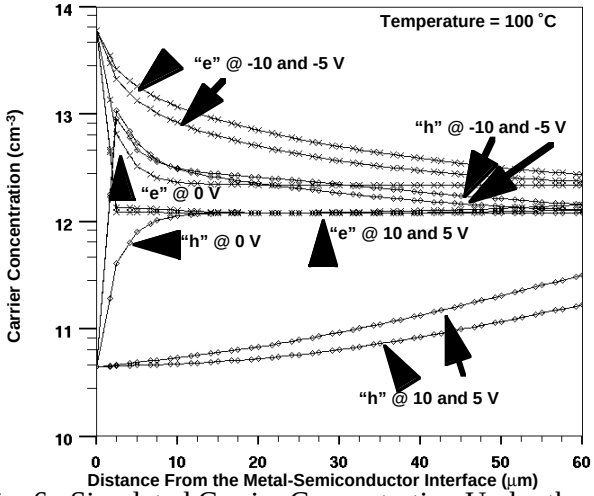

Fig. 6. Simulated Carrier Concentration Under the Conductor for Various Bias Conditons at 100 ˚C

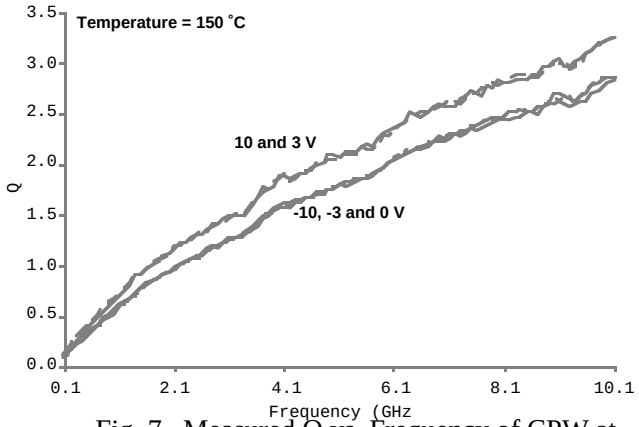

Fig. 7. Measured Q vs. Frequency of CPW at Various Bias Conditions at 150˚C

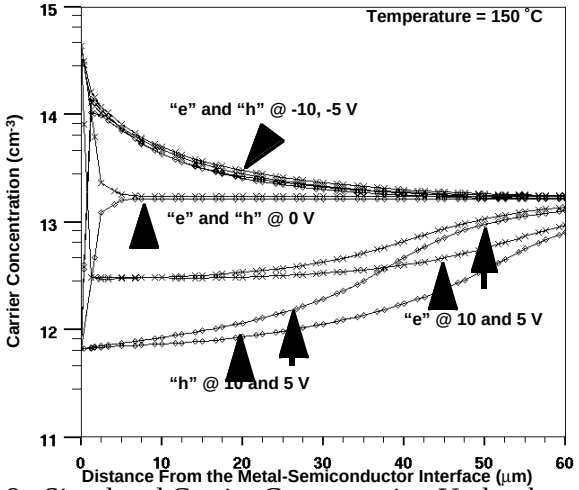

Fig. 8. Simulated Carrier Concentration Under the Conductor for Various Bias Conditons at 150 ˚C